ABSTRACT OF THE DISCLOSURE

A test pattern generator and a method of generating a test pattern. The method includes converting a test pattern into a program and simulating the program to produce a test pattern. The test pattern is applied to a test circuit to obtain simulated test results. The program is written to a memory unit. The test circuit is tested using the program inside the memory unit to produce actual test results. The simulated test results and the actual test results are compared. If the simulated and the actual results match each other, the test circuit is repeatedly test using the test pattern until no delay between loop backs is found. However, if there is a mismatch between the simulated and the actual results, the program is adjusted and the test circuit re-tested until a match between the simulated results and the actual results is found.